A Scaling Study of Excess OFF-State Current in InGaAs Quantum-Well MOSFETs

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***Abstract*— A scaling study of excess OFF-state current in planar InGaAs quantum-well MOSFETs is reported. We find that pure band-to-band tunneling (BTBT) dominates the drain OFF-state current in devices with channel length above ~1 μm. In this regime, the drain–gate voltage sets the rate of BTBT. In devices with channel lengths below 1 μm, a parasitic bipolar transistor effect becomes relevant. The bipolar current gain is found to scale inversely with the effective channel length for Lg between 70 nm and 1 μm, as expected from simple bipolar transistor theory. For Lg below ~70 nm, the OFF-state current increases rapidly due to an enhancement in bipolar current gain as a result of strong short-channel effects and punchthrough. Current gains in excess of 104 have been observed. A reduction in channel thickness decreases both BTBT and the bipolar gain effect.**

***Index Terms*— III–V, band-to-band tunneling (BTBT), bipolar effect, floating-body, MOSFETs, punchthrough, quantum well (QW), self-aligned.**

I. Introduction

THE InGaAs quantum-well MOSFET (QW-MOSFET) is considered a promising alternate device structure for future CMOS applications because of superior electron transport properties in the InGaAs channel [1], [2]. To reduce device footprint and improve on-state performance, i.e., current drive and transconductance, tight self-alignment is required with the heavily doped source and drain placed closely aligned to the gate edges. The on-state performance further improves by increasing the InAs content in the channel [3]–[5]. When scaled to very small dimensions, self-aligned InGaAs MOSFETs with a high InAs channel composition exhibit excess OFF-state drain-to-source leakage current that prevents the transistors from being effectively turned off [6]–[8]. Initial observations of this effect were made in planar MOSFETs but similar issues have been recently diagnosed in FinFETs [9] and gate-all-around nanowire FETs [10].

Initial experimental studies in planar InGaAs MOSFETs noted that the excess OFF-state current carries the signature of band-to-band tunneling (BTBT) [6]. BTBT has been well studied in silicon MOSFETs and it has a physical origin in a direct tunneling process at the drain edge of the channel [11], [12]. With the gate voltage below threshold and a high drain voltage, a large electric field appears at the drain end of the channel that leads to elastic tunneling of valence electrons in the channel to the conduction band in the drain. There have now been several claims of observation of BTBT in InGaAs MOSFETs, and various engineering techniques have been studied to mitigate it [6]–[8].

The phenomenon known as gate-induced drain leakage has been extensively studied in floating-body silicon-on-insulator (SOI) MOSFETs [11]–[14]. In these devices, a parasitic bipolar effect was identified that amplifies BTBT or impact ionization current generated by the high gate-to-drain field [14]–[16]. An n-type MOSFET contains a parasitic n-p-n bipolar junction transistor (BJT) where the body acts as base, source as emitter, and drain as collector. With a floating body, the base of the BJT is open and holes generated at the drain end of the channel pile up in the body and eventually turn on the base–emitter junction of the BJT. In this manner, the hole generation current is multiplied by the current gain of the parasitic bipolar transistor, resulting in a large emitter (drain) electron current [17]. Similar bipolar effects have been observed in other transistors such as planar FETs and FinFETs on SiGe and Ge [18], [19].

QW InGaAs MOSFETs also feature a floating body. As in floating-body SOI MOSFETs, a parasitic bipolar transistor has been found to amplify the BTBT current with the current gain scaling as L_g^{-1} [20], [21]. In InAs-rich InGaAs MOSFETs in the sub-100-nm gate length range, gains as high as 10^3–10^4 have come to be expected from the simulations [20], [21].

In spite of its relevance, to date, there has yet to be published a detailed scaling study of BTBT-induced OFF-state current in the experimental InGaAs MOSFETs with different gate lengths, channel thickness (t_c), and under different bias conditions. A complicating factor in these studies is the relatively high gate-leakage current density characteristic of device designs with aggressively scaled gate dielectric as required to achieve good on-current performance and short-channel effects (SCEs). Gate leakage tends to dominate source-to-drain

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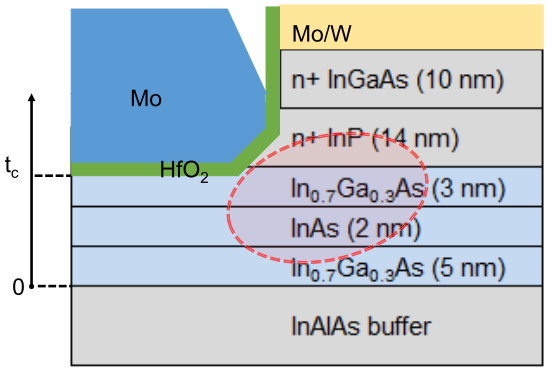

Fig. 1. Cross-sectional schematic of the InGaAs MOSFET studied in this paper. The gate edge of the device on the drain side is depicted. The heterostructure is specified with the layer thickness in parenthesis. Unless indicated, the ternary semiconductor compositions are lattice matched to InP. The region where BTBT takes place is colored in red.

leakage in long-channel devices complicating a thorough study of excess OFF-state current. Also, to date, devices with a limited channel length range ($L_g \leq 500$ nm) have been studied [6], [20], with the consequence that BTBT and the bipolar gain effect could not be cleanly separated.

In this paper, we fabricate InGaAs MOSFETs with a relatively thick gate dielectric, as compared with our previous high-performance devices [6], [20]. This allows us to suppress gate leakage and carry out a systematic study of excess InGaAs OFF-state current across a broad range of L_g, t_c, and bias. The devices studied here cover L_g from 70 nm to 8 μm, and t_c from 5 to 9 nm. We find that pure BTBT, dominant in long-channel devices, exhibits a classic dependence on the gate-to-drain voltage difference and is relatively independent of channel thickness. As the gate length shortens below about 1 μm, the BTBT current is multiplied by the bipolar current gain which increases as L_g is shortened and is suppressed by a thinner channel. In this regime, the voltage dependence of the OFF-state current also changes.

This paper is organized as follows. The device structure and fabrication process are presented in Section II. An analysis of BTBT in long-channel devices is described in Section III. Bipolar amplification in scaled QW-MOSFETs and its dependence on L_g, t_c, and bias are discussed in Section IV. This is followed by the conclusions.

II. Experiment

The InGaAs QW-MOSFETs studied here are fabricated using a self-aligned process described in detail elsewhere [22]. A schematic of the gate–drain region describing the heterostructure [grown on InP by molecular beam epitaxy (MBE)] is shown in Fig. 1. The as-grown composite channel comprises of strained InGaAs/InAs/InGaAs layers with a total thickness of 10 nm. The layers labeled with "n^+" are doped with silicon to $N_D = 3 \times 10^{19} - 4 \times 10^{19}$ cm^{-3}. This is to facilitate a low-resistance nonalloyed ohmic contact using molybdenum (Mo) [23]. The high-k metal gate stack consists of HfO_2 and Mo. The gate dielectric HfO_2 is grown by atomic layer deposition at 250 °C and its thickness is 4 nm. This is 60% thicker than in our previous high-transconductance short-channel QW-MOSFETs [22]. With thicker HfO_2, gate leakage is significantly reduced, and a clearer picture of excess OFF-state current emerges.

In our InGaAs MOSFET, the gate stack is nested in a self-aligned manner inside the gate recess which is produced through a combination of dry etch and digital etch [22], [24]. The gate recess technology employed here has demonstrated an ability to control the channel thickness (t_c) in the intrinsic device within 1 nm with extremely small surface roughness comparable to that of the as-grown MBE wafer [22]. As indicated in Fig. 1, we label t_c as the distance between the oxide–semiconductor interface and the bottom of the InGaAs channel layer. Three values of t_c from 5 to 9 nm were investigated in this paper. All transistors (with different t_c) used in this paper were fabricated out of the same wafer following an identical process flow. The only difference is the number of digital etch cycles used in the gate recess step. Therefore, all transistors are identical except for the depth of the recess, i.e., the intrinsic channel thickness.

The devices are isolated from each other by a 40-nm deep mesa etched into the InAlAs buffer layer by means of an H_2O_2-based wet etch. The current through two isolated mesas is verified to be smaller than 10 pA at 1 V. This is significantly smaller than any terminal current measured in this paper.

Devices with effective channel lengths (L_g) between 70 nm and 8 μm were fabricated. L_g is the distance between the two gate edges and is calibrated using SEM cross-sectional image. All devices have a width of 10 μm. The device has an overlapped structure with metal gate covering part of the n^+ InP ledge. The length of the n^+ InP ledge is about 15 nm.

I–V measurements were taken as follows. The gate voltage was swept in a range of about 1.5 V and with increasing V_{ds} from 50 mV to 0.7 V. Care was exercised not to damage the devices nor induce any significant V_t shifts due to gate oxide trapping [25].

Fig. 2(a) shows the subthreshold characteristics of $t_c = 9$ nm devices over the full range of L_g at $V_{ds} = 0.5$ V at room temperature. The x-axis in Fig. 2(a) is $V_{gt} = V_{gs} - V_t$, where V_t is the threshold voltage. We analyze our data this way because we find that V_t varies in devices with different channel lengths due to SCEs. V_t also changes with drain bias due to drain-induced barrier lowering. V_t is defined as the value of V_{gs} for which I_d. L_g product is constant and equal to 1 μA, where I_d represents the current density normalized by the device width.

In Fig. 2(a), below the threshold, excess OFF-state current is clearly observed in all devices. In long-channel devices, the excess drain current, I_d, is relatively independent of L_g. The OFF-state current becomes more prominent and increases as L_g is scaled down in short-gate-length devices. Across the full-voltage span and for all devices, the magnitude of the OFF-state drain current is much higher than the gate current. In the worst case of very long-channel length [$L_g = 8$ μm, black lines in Fig. 2(a)], the ratio of I_d/I_g is >10 across the relevant V_{gt} range.

Fig. 2(b) shows the minimum saturated subthreshold swing (S) at $V_{ds} = 50$ mV as a function of L_g. The significant increase of S for $L_g < 250$ nm is the result of SCE.

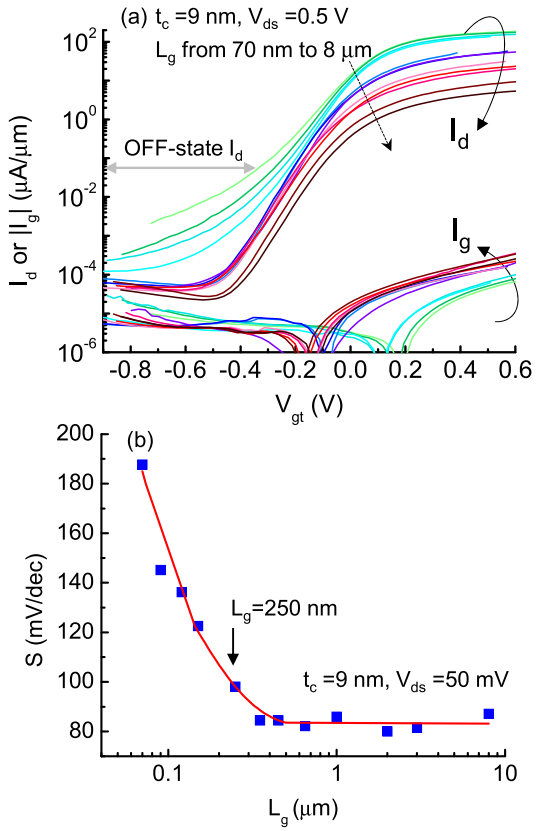

Fig. 2. (a) I_d and I_g versus V_{gt} for devices with L_g of 70, 90, 120, 150, 250, 350, 450, and 650 nm, and 1, 2, 3, and 8 μm (color from light green to black). The transistor is biased in saturation with drain bias of 0.5 V. The x-axis is $V_{gt} = V_{gs} - V_t$ where V_t is defined in the text. (b) Minimum subthreshold swing ($V_{ds} = 50$ mV) as a function of L_g. For both figures, $t_c = 9$ nm.

III. BTBT in Long-Channel Devices

The origin of excess OFF-state drain current in the absence of a bipolar gain effect is a BTBT process at the drain edge of the gate. The standard BTBT model is derived from the Wentzel–Kramer–Brillouin approximation, which is given by

$$I_{\mathrm{BTBT}} = AE_s \exp\left(-\frac{\pi m^{*1/2} E_g^{3/2}}{2\sqrt{2}q\hbar E_s}\right) \quad (1)$$

where A is a prefactor, E_s is the surface electric field, m^* is the tunneling effective mass, and E_g is the energy gap [26]. Equation (1) can be written in a simplified manner as

$$I_{\mathrm{BTBT}} = AE_s \exp\left(-\frac{B}{E_s}\right) \quad (2)$$

where B captures all the terms in the exponent except for E_s.

The surface electric field, E_s, can be expressed, to the first order, as [6], [19][1]

$$E_s = \frac{V_{\mathrm{dg}}}{\frac{\varepsilon_{\mathrm{ch}}}{\varepsilon_{\mathrm{ox}}} t_{\mathrm{ox}}}. \quad (3)$$

[1]In [11], the expression for E_S includes a term on $-E_g/q$, where E_g is the bandgap of the channel. This accounts for the electrostatic potential difference between threshold and flatband in a conventional n-type MOSFET on a p-type substrate. In the QW-MOSFETs studied in this paper, the channel is undoped and we can assume that E_s at threshold is negligible. It is because of this that E_S in (3) does not include a bandgap term.

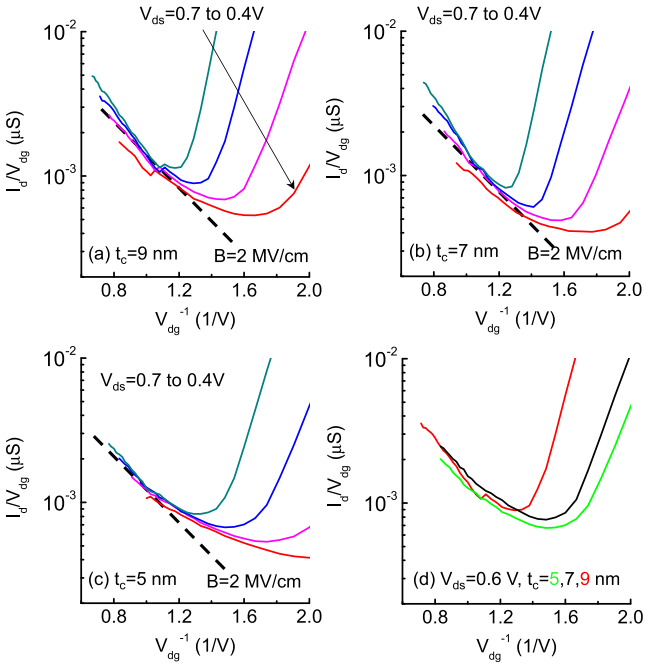

Fig. 3. Semilogarithmic plot based on (2) for $L_g = 8$ μm devices with (a) $t_c = 9$ nm, (b) $t_c = 7$ nm, and (c) $t_c = 5$ nm. The data are extracted from the I_d–V_{gs} measurement for V_{ds} from 0.4 to 0.7 V. The dashed line indicates the case when B is 2 MV/cm in (2). (d) Semilogarithmic plot based on (2) for varying t_c from 5 to 9 nm and at the fixed V_{ds} of 0.6 V. The lines overlap at high V_{dg}.

Prior experiments on devices with $L_g = 500$ nm revealed that the excess OFF-state current follows the temperature and bias trends that are expected for BTBT and that are embodied in (1)–(3) [6]. As the temperature decreases, the bandgap of the semiconductor increases. In consequence, the BTBT current drops exponentially as $E_g^{3/2}$ (1). In addition, the BTBT current increases quickly with V_{dg} through (1) and (3). However, this paper will show, at $L_g = 500$ nm, the bipolar gain effect can be sizable. One has to get to $L_g = 8$ μm devices to see negligible gate length dependence and, therefore, contemplate a pure BTBT behavior.

Following (2) and (3), Fig. 3(a)–(c) shows I_d/V_{dg} versus $1/V_{\mathrm{dg}}$ in semilog plot for different values of V_{ds} for $L_g = 8$ μm devices with three-channel thicknesses. According to (2) and (3), I_d/V_{dg} should only depend on the absolute value of V_{dg} regardless of the individual values of V_d and V_g. Also, in a semilog plot, this dependence should be linear. Indeed, these trends are observed in Fig. 3(a)–(c) for all channel thicknesses, although some deviation from the straight line is observed at high OFF-state current (toward the top left of the plot). This could be due to migration of the BTBT region at higher V_{dg} from the InAs core toward the top InGaAs layer closer to the gate.

The parameter B in (2) can be extracted from the data shown in Fig. 3. The extracted value of B is between 2 and 2.5 MV/cm, relatively independent of V_{dg} or t_c. Based on established bulk values of effective mass and bandgap as a function of InAs composition [26], the theoretical value of B is calculated to be about 2 MV/cm for InAs. The mechanical strain and carrier confinement in the thin body channel are expected to increase both the effective mass and

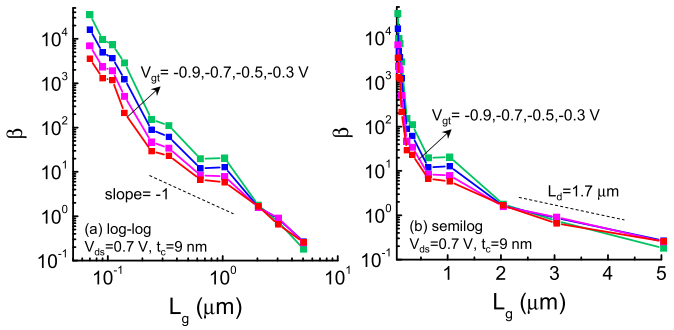

Fig. 4. Bipolar gain β as a function of L_g from 70 nm to 5 μm at $V_{ds} = 0.7$ V in log–log (left) and semilog scale (right). Different values of V_{gt} are given.

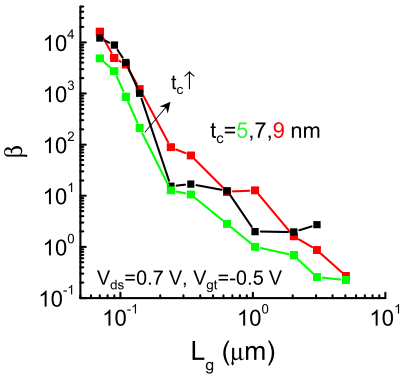

Fig. 5. Bipolar gain β as a function of L_g for L_g from 70 nm to 5 μm at $V_{gt} = -0.5$ V and $V_{ds} = 0.7$ V. Channel thickness is varying.

the bandgap. The value of $B = 2$ MV/cm should be considered a lower bound.

Fig. 3(d) shows I_d/V_{dg} versus $1/V_{dg}$ at $V_{ds} = 0.6$ V for $L_g = 8$ μm devices with three different channel thickness. We find that the BTBT current is relatively independent of t_c. This is consistent with 2-D TCAD simulations in our previous work that indicate that the high-field responsible for BTBT develops in the access region beneath the n^+ cap right next to the gate [20]. In this region, the extrinsic channel thickness is identical in all devices and equal to 10 nm.

IV. Parasitic Bipolar Effect

As observed in Fig. 1, for short-gate length devices, I_d in the OFF-state increases as L_g scales down below about 1 μm. This is due to the current gain of the parasitic bipolar transistor, β, that strongly depends on L_g. We can extract β by normalizing the OFF-state leakage current to the BTBT current measured in the longest channel device ($L_g = 5$ μm) at the same bias. Following simple bipolar transistor theory, in the presence of BTBT in the OFF-state, we expect that

$$I_d = I_{BTBT}(\beta + 1). \tag{4}$$

An assumption made here is that the BTBT current is unaffected by the bipolar gain effect, or, in other words, that the modulation of the source-to-channel barrier height ($\Delta\varphi_b$) does not impact the field at the drain end of the channel. We have verified through simulations that this is indeed the case in the absence of significant SCE [20], [21].

Fig. 4 shows the extracted β versus L_g for $t_c = 9$ nm devices at a fixed $V_{ds} = -0.7$ V and various values of V_{gt}. Fig. 4(left) shows the extracted β in log–log scales and the Fig. 4(right) shows the graph of the same data in a semilog scale. Three regimes can be distinguished, depending on the value of L_g. There is an intermediate regime, for L_g between 0.25 and 1 μm, in which β is found to be inversely proportional to L_g, just as expected from classic BJT theory [17].

For $L_g < 250$ nm, the current gain scales faster than L_g^{-1}. This can be the result of strong SCEs in scaled devices, particularly, due to the relatively thick gate oxide. A clear indication of the SCE is the increase in subthreshold swing shown in Fig. 2(b). For the shortest gate length ($L_g = 70$ nm) at small $|V_{gt}|$, a huge current gain, larger than 10^4, is observed. This is about 100 times higher than the bipolar gains reported in InGaAs FinFETs [9] or nanowire FETs [10] at comparable gate length.

There is a voltage dependence for β that is opposite to that of BTBT: as the gate voltage shifts negative, β shrinks. This is consistent with well-known bipolar transistor physics in which β is reduced as the base doping increases due to the enhancement of the energy barrier between emitter and base. This was also confirmed in our previous simulations [21].

For $L_g > 1$ μm, Fig. 4(a) shows that as L_g increases, the bipolar gain drops more rapidly than L_g^{-1}. This is expected when the BJT base width (L_g in our case) becomes comparable to the minority carrier diffusion length in the same region (L_d) and base recombination becomes significant. In this regime, we expect a β dependence as $\sim\exp(-L_g/L_d)$. Indeed, the semilog scale on the right shows this. From the slope of the β decay with L_g, a value of $L_d = 1.7$ μm can be extracted. L_d shows negligible dependence on the gate bias.

Channel thickness is found to also impact the bipolar current gain. Fig. 5 shows that as the channel is made thinner, β drops. The impact of channel thickness arises from the following mechanisms. When the channel is turned off, the energy band alignment is such that electron injection from the source into the channel preferentially takes place toward its bottom. In consequence, the source-to-channel potential barrier for electrons is more weakly controlled by the gate in thicker channels, yielding a higher β for the parasitic BJT. This was discussed in the simulations in [21].

V. Conclusion

This paper investigates the physics behind excess OFF-state current in InGaAs QW-MOSFETs with different gate lengths and channel thickness. The origin of the OFF-state leakage is BTBT coupled with a bipolar gain effect. For channel lengths above 1 μm, the OFF-state current is dominated by BTBT at the drain end of the channel. The parasitic bipolar effect affects the OFF-state leakage for channel lengths below 1 μm. The bipolar current gain exhibits a strong gate length dependence with three different regimes. In very short-channel devices, current gains in excess of 10^4 have been extracted. This is significantly higher than in InGaAs nanowire FETs or FinFETs. Channel thickness reduction is shown to reduce the bipolar gain.

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